Remarks

Applicant thanks the Examiner in advance for a careful examination and allowance of this application.

The specification amendments conform to those made in the earlier applications.

New claims 25-63 better define the claimed inventions.

The enclosed Petition to Make Special explains the grounds for the petition in accordance with the rules.

The enclosed Information Disclosure Statement A briefly discusses the art cited on the electronically filed IDS-A and the enclosed PTO-1449 forms.

Support for claim limitations

Some claim limitations find support in the present application through incorporation by reference of portions of US 5,001,713. That patent issued from Application No. 07/308,272, filed February 8, 1989. The present application as filed included this incorporation by reference. See the original application, page 11, end of the first paragraph.

The present application provides a disclosure of the Event Qualification Module, EQM, 32 in Figure 7. This supports the claim limitations of the "event control circuit." The present application concludes the description of the structure depicted in Figure 7 by saying: "The operation and protocol of the Event Qualification Module are described in" the cited US 5,001,713 and US 5,103,450.

In Figure 6 of US 5,001,713, the drawing depicts control register 88, which supports the "protocol selection memory" of claims 25, 39, and 53.

In Figures 6 and 7 of the incorporated patent, the drawings depict leads C0 and C1, which carry the protocol selection signals to the EQM. One of these signals supports "a protocol selection signal" of claims 25 and 39.

At Column 11, Line 47, the incorporated patent says: "The C0 and C1 inputs come from two scannable bits in the EQM control register 88. C0 and C1 provide the required two-bit command input for the EQM controller to perform one of four event qualification operations described below."

At Column 9, Line 45, the incorporated patent says: "The SDI signal is input to a control register 88. The control register 88 outputs signals C0, C1 and I/E to an EQM controller 90." The I/E signal supports the "an enable signal register" of claims 37, 51, and 63.

In the present application, Figure 7, the EXPDAT0-15 leads support the limitation of "plural expected data input leads" in claims 28, 42, and 56.

In Figure 6 of the incorporated patent, a start and stop expected data section 98 supports the limitation of "an expected data memory". In the incorporated patent, column 9, line 63, the text says: "The start expected data register 100 and stop expected data register 102 are connected to a multiplexer 114, which outputs the signal EXPDAT." This is the same signal EXPDAT0-15 depicted in Figure 7 of the present application.

The claims

Independent claim 25 defines an integrated circuit comprising functional circuits, a serial data input lead and a serial data output lead, at least one serial scan path of scan registers.

The scan registers of the serial scan path are coupled between the serial data input lead and the serial data output lead. The serial scan path is coupled to the functional circuits.

A protocol selection memory is coupled to the serial scan path. The protocol selection memory has at least one storage location to store a protocol selection signal.

An event control circuit is coupled to the serial scan path. The event control circuit includes a protocol input connected to the protocol selection memory, an event input lead and an event output lead.

Independent claim 39 defines observation circuits comprising a serial scan signal input lead, a serial scan signal output lead, a serial clock signal input lead, a mode select signal input lead, and a serial scan path coupled between the serial scan signal input lead and the serial scan signal output lead.

An access port circuit is coupled to the serial scan path, the mode select signal input lead, and the serial clock signal input lead.

A protocol selection memory is coupled to the serial scan path and includes at least one storage location to store a protocol selection signal.

An event control circuit has a protocol input coupled to the protocol selection memory, an event input lead, and an event output lead.

Independent claim 53 defines an integrated circuit comprising a functional circuit, a serial data input lead

and a serial data output lead, a serial scan path of scan registers coupled between the serial data input lead and the serial data output lead, a scan clock signal lead and a scan mode signal lead, and an event input lead.

An access port has a first input coupled to the scan clock signal lead, a second input coupled to the scan mode signal lead, and at least one control output coupled to the serial scan path.

A protocol selection memory is coupled to the serial scan path and has at least one storage location.

Event control circuitry has an input coupled to the event input lead, an input coupled to the protocol selection memory, and an output coupled to the functional circuit.

Selected art

Applicant relies upon the combination of all the limitations in the independent claims for patentability and not any general description.

Independent claims 25, 39, and 53 distinguish over the cited art by requiring: a serial data or scan signal input lead; a serial data or scan signal output lead; a serial scan path coupled between the serial input lead and the serial output lead; a protocol selection memory coupled to the serial scan path; and an event control circuit coupled to the protocol selection memory.

The following cited art fails to disclose a protocol selection memory coupled to a serial scan path in the defined combinations.

Applicant could repeat a statement of these distinguishing limitations after the discussion of each following cited patent to meet the requirements of 37 CFR 1.111(b) and (c). Since each cited patent and the cited patents in combination fail to teach or suggest these distinguishing limitations, applicant will rely upon the preceding statement of the distinguishing limitations, without repetition.

US Patents

US 4,023,142 to Woessner discloses a common reliability and service bus connected to each functional unit of LSI apparatus. The bus provides for an addressed unit to go through an operation after a test pattern has been loaded into the unit while the system continues to operate concurrently. Figure 4 depicts a control system adapter 200 with shift register configuration 210. Data bits 0-7 appear to be loaded in parallel into Diagnostic Address Register 175, Mode Register 1 120, Mode Register 2 180, Mode Register 3 185, and Shift Register 170. Level Shifting Serial Design latches 210 form a scan path. An exclusive OR circuit 400 compares the data from shift register 210 to be compared serially, bit-by-bit, with an expected data pattern loaded into register 170.

US 4,108,359 to Proto discloses a device for detecting errors in the execution of a sequence of coded instructions. A feed-back shift register generates a digital sequence combined with the sequence of instructions to compute a unique sequence check word that is compared to a stored, known good check word. This patent was cited in parent patent US 5,905,738.

US 4,268,902 to Berglund, et al. discloses a maintenance interface for interfacing a service processor and a central processor operating synchronously to each other. The interface circuitry synchronizes the service processor to the central processing unit and decodes commands from the service processor. The interface circuitry also establishes communication from the central processing unit to the service processor and resolves communication contention between the processors.

Circuitry provides independent control of the clocks to each functional unit or shift ring (scan path) and the functional unit interface signals to other functional units or arrays. The interface includes a Level Sensitive Scan Design (LSSD) testing system with four separate shift rings and provides degating of central processing unit interfaces as required for this testing approach.

US 4,312,066 to Bantz, et al. discloses an interface between a host processor and a diagnostic/debugging processor that troubleshoots the hardware and software of the host processor. The host uses the Level Sensitive Scan Design rules.

The disclosed system allows the machine state and memory of the Host CPU to be captured at the end of an instruction or at the end of a cycle. It further allows selective reading and writing of the memory state by conditioning the H-machine with state information that will cause words from or to memory to be transferred to the D-machine. The system allows control over interruption, channel activity and address translation and provides a diagnostic CPU with its own memory to perform diagnostic and debug functions.

US 4,504,784 to Goel, et al. discloses chips in a module or any second level package. The test mechanism built into each chip will be used in place of mechanical probes to perform a chip-in-place test and interchip wiring test of the package. Level sensitive scan design rules need to be used for each chip and for the package clock distribution network. Divisional patent of US 4,441,075 and corresponds to US 4,494,066. This patent was cited in parent patent US 5,905,738.

US 4,514,845 to Starr discloses locating a bus fault by placing devices in a high impedance state and sensing current flow between devices. This patent was cited in parent patent US 5,905,738.

US 4,628,511 to Stitzlein, et al. discloses recording pre- and post-failure events to analyze signal activity on an input/output channel to determine failing equipment. This patent was cited in parent patents US 5,905,738 and US 6,131,171.

US 4,674,089 to Poret, et al. discloses an in-circuit emulator (ICE). Capture logic 15 captures the contents of the program address register (PAR), the internal data bus (IDB), and various microprocessor 13 control (CONTROL) lines. The capture logic 15 provides outputs on lines 45 to trace circuits 25. Trace circuits 25 use a FIFO buffer to transfer the captured data to the output pins 31 of the chip 11. A content addressable memory 17 and a software programmable logic array 21 operate as a finite state machine to perform testing. The content addressable memory 17 determines the status of the processor and compares it with a set of four possible word recognizers with comparators 61. The content addressable memory 17 and software programmable logic array

are apparently loaded from the microprocessor 13 over lines 41 through mode control 27 and lines 43.

US 4,701,920 to Resnick, et al. discloses built-in self test circuitry 10 for LSI circuit chips. The test circuitry includes a serial scan path (TDI-TDO) and control signal logic 42. Input register 36 applies test signals to the main logic function 14 and output register 38 receives output signals from the main logic function 14.

US 4,817,093 to Jacobs, et al. discloses testing a multi-chip packaged structure by isolating the one chip under test, applying test signals to that chip, creating a signature of the response signals from that chip and comparing the signature to that of a known good chip. This patent was cited in parent patent US 5,905,738.

US 4,887,267 to Kanuma discloses a logic circuit having a FIFO memory circuit to store values from a test node. The FIFO memory then is unloaded to trace the outputs of such as the states of an internal bus. This patent was cited in parent patent US 5,905,738.

US 4,926,425 to Hedtke, et al. discloses a system for testing successive component groups separated by accessible nodes. The process observes data at the nodes and supplies test data to the nodes. This patent was cited in parent patent US 5,905,738.

US 4,947,357 to Stewart, et al. discloses a circuit board carrying plural integrated circuits, each with an internal scan chain. The scan input of each integrated circuit is connected to a system scan controller 26. The scan outputs of the integrated circuits are connected to

multiplexer 30 for selective testing of individual integrated circuits.

US 5,084,874 to Whetsel discloses a testing buffer register 12. See Figure 2. The test cell can also include compare and other logic. See Figures 6 and following. Corresponds to US 5,495,487; US 5,602,855; US 5,631,911; US 6,081,916; US 6,304,987; and US 6,611,934. This patent was cited in parent patent US 5,905,738.

This patent is believed to be not prior art to the present application. This patent is to the same inventor as in this application and issued on January 28, 1992, after the filing date of June 30, 1989 of the present application.

Other Documents

The Intel 80386 Programmer's Manual discloses the debugging features of the 80386 architecture and the registers used for debugging. The principal debugging support takes the form of debug registers. The debug registers support both instruction breakpoints and data breakpoints. A reserved debug interrupt vector permits the processor to automatically invoke a debugger task or procedure when an event occurs that is of interest to the debugger. The debug registers are accessed by variants of the MOV instruction.

The Intel Microprocessor and Peripheral Handbook discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE

INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

The Intel Microprocessor and Peripheral Handbook, Section 2.11.2 TLB Testing, also discloses that there are two TLB (Translation Lookaside Buffer) testing operations. One is to write entries into the TLB. The other is to perform TLB lookups. C: is the command bit. A "0" written into this bit causes an immediate write into the TLB entry. A "1" written into this bit causes an immediate TLB lookup.

The Intel386™ DX Microprocessor data sheet discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

In Section 2.11.2 TLB Testing, when testing, the Translation Lookaside Buffer must be turned off (PG=0 in CRO) to enable the TLB testing hardware and avoid interference with the test data being written to the TLB. There are two TLB testing operations: 1) write entries into the TLB, and 2) perform TLB lookups. Two Test Registers, shown in Figure 2-12, are provided for the purpose of testing. TR6 is the "test command register", and TR7 is the "test data register". Figure 2-12 depicts the fields within the registers.

C: is the command bit. For a write into TR6 to cause an immediate write into the TLB entry, write a 0 into this bit. For a write into TR6 to cause an immediate TLB lookup, write a 1 to this bit.

The Joint Test Action Group paper, January, 1988, discloses an early version of the standard for a boundary scan test architecture.

The Kuban paper discloses a built-in self-test of a Motorola microprocessor having a serial architecture. The self-test is based on a ROM-driven signature analysis technique. The resulting signature is output from the microprocessor for external examination of the signature.

Referring to Figure 9 and the description on page 39, right-hand column, the operating mode of the MC6804P2 is controlled by RESET, MDS, PA7, and PA6. When RESET is brought high, the levels on the MDS, PA7, and PA6 pins are sampled, and the appropriate mode is selected. The two test modes are invoked by a high on the MDS and PA7 pins. The functional test is then entered if the PA6 pin is low; otherwise, a high on PA6 invokes the ROM verify test. The self-test fixture provides a good/bad indicator for the ROM verify test.

The Whetsel (January, 1988) paper discloses an overview of the JTAG IC test architecture. The disclosed architecture is readily expandable to accommodate boundary scan and other IC test structures such as built-in self test (BIST) and internal core scan design. Figure 8 depicts a boundary register bit.

Conclusion

Claims 25 through 63 are allowable.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests allowance of this application.

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